AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (PREVIOUSLY PRESENTED) An apparatus comprising:

a first input configured to receive a clock signal;

a second input configured to receive a data signal having a first setup/hold window with respect to a transition of said clock signal;

a first circuit configured to (i) receive said data signal from said second input and (ii) present a delayed data signal having a second setup/hold window with respect to said transition of said clock signal, wherein (i) a difference between said first setup/hold window and said second setup/hold window is configured in response to one or more of a plurality of delay times, (ii) each of said plurality of delay times is less than a period of said clock signal and (iii) said plurality of delay times provides a user configurable delay of said second setup/hold window relative to said transition of said clock signal; and

a second circuit configured to receive said delayed data signal from said first circuit and said clock signal from said first input.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein:

said second circuit is configured to present a data output in response to said delayed data signal and said clock signal.

3. (PREVIOUSLY PRESENTED) The apparatus according to claim 2, wherein said second circuit comprises a register that is further configured to store said delayed data signal in response to said clock signal.

4. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said first circuit further comprises a high speed transceiver logic (HSTL) circuit configured to present a first signal in response to said data signal.

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 4, wherein said first circuit further comprises one or more delay circuits each configured to present an output delay signal in response to said first signal.

6. (PREVIOUSLY PRESENTED) The apparatus according to claim 5, wherein said first circuit further comprises a switch configured to receive said one or more output delay signals and present said delayed data signal.

7. (ORIGINAL) The apparatus according to claim 6, wherein said switch is further configured in response to a user configuration signal.

8. (ORIGINAL) The apparatus according to claim 7, wherein said user configuration signal comprises a setup and hold timing configuration signal.

9. (ORIGINAL) The apparatus according to claim 7, wherein said user configuration signal comprises a programmable signal.

10. (ORIGINAL) The apparatus according to claim 7, wherein said user configuration signal comprises a multi-bit signal.

11. (PREVIOUSLY PRESENTED) An apparatus comprising:

means for receiving (i) a clock signal and (ii) a data signal having a first setup/hold window with respect to a transition of said clock signal;

means for presenting a delayed data signal having a second setup/hold window with respect to said transition of said clock signal in response to said data signal, wherein (i) a difference between said first setup/hold window and said second setup/hold window is configured in response to one or more of a plurality of delay times, (ii) each of said plurality of delay

times is less than a period of said clock signal and (iii) said plurality of delay times provides a user configurable delay of said second setup/hold window relative to said transition of said clock signal; and

means for storing said delayed data signal in response to said clock signal.

12. (PREVIOUSLY PRESENTED) A method for programming a setup/hold window, comprising the steps of:

(A) receiving (i) a clock signal and (ii) a data signal having a first setup/hold window with respect to a transition of said clock signal; and

(B) presenting (i) a delayed data signal (a) having a second setup/hold window with respect to said transition of said clock signal and (b) generated in response to said data signal to a first input of a circuit and (ii) said clock signal to a second input of said circuit, wherein (i) a difference between said first setup/hold window and said second setup/hold window is configured in response to one or more of a plurality of delay times, (ii) each of said plurality of delay times is less than a period of said clock signal and (iii) said plurality of delay times provides a user configurable delay of said second setup/hold window relative to said transition of said clock signal.

13. (PREVIOUSLY PRESENTED) The method according to claim 12, further comprising the steps of:

(C) storing said delayed data signal and presenting a data output signal in response to said clock signal.

14. (CANCELED)

15. (PREVIOUSLY PRESENTED) The method according to claim 12, wherein step (B) further comprises presenting a first signal in response to said data signal.

16. (ORIGINAL) The method according to claim 15, wherein step (B) further comprises presenting one or more output delay signals in response to said first signal.

17. (PREVIOUSLY PRESENTED) The method according to claim 16, wherein step (B) further comprises receiving said one or more output delay signals and presenting said delayed data signal.

18. (PREVIOUSLY PRESENTED) The method according to claim 17, wherein step (B) further comprises switching said one or more output delay signals in response to a user configuration signal.

19. (PREVIOUSLY PRESENTED) The method according to claim 18, wherein said user configuration signal comprises one or more of (i) a setup and hold timing configuration signal and (ii) a multi-bit signal.

20. (ORIGINAL) The method according to claim 18, wherein said user configuration signal comprises a programmable signal.

21. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein a total of all of said plurality of delay times is less than said period of said clock signal.

22. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, further comprising a first-in-first-out (FIFO) memory.

23. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said data signal and said clock signal are externally generated.